AN2168
Application note

ST10F27x hardware development
Getting started

Introduction

The ST10F27x MCUs are derivatives of the STMicroelectronics ST10 family of 16-bit CMOS microcontrollers. They combine high CPU performance (CPU frequency up to 64 MHz) with high peripheral functionalities and enhanced I/O-capabilities. They offer on-chip high speed single voltage Flash memory, on-chip high speed RAM and support clock generation via PLL or an external clock. The ST10F27x MCUs also provide an enhanced 16-bit DSP co-processor to improve their performance in signal processing algorithms.

This application note complements the *ST10F27x datasheet* and *user manual* by describing the minimum hardware environment required to build an application around the ST10F27x. A number of features of the ST10F27x devices are described in the first five chapters. In the sixth, a basic schematic is given illustrating the minimum hardware required to get the ST10F27x running. For a deeper description of these features, refer to the *ST10F27x datasheet* or *user manual*.

In order to build an application around ST10F27x, the application board should, at least, provide the following features:

- Power supply
- Clock management
- Reset control
- Boot mode settings

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1 Power supply

1.1 Overview

The ST10F27x devices are processed in 0.18 µm technology. ST10F27x core logic and I/O peripherals need different power supplies. In fact, ST10F27x core logic operates with an 1.8V power supply while the I/O peripherals operate with a power supply in the 4.5V to 5.5V range.

The ST10F27x devices are single supply. This means that just one external supply of 5V is necessary to feed both core and peripherals. The power management block includes a regulator to provide the core logic 1.8V supply from the 5V input supply.

The internally generated 1.8V supply is available on pin V18 (pin 56) of the ST10F27x. **No external supply can be connected to V18**. A decoupling ceramic capacitor of a typical value 10nF(max 100nF) has to be connected between the V18 pin and the nearest Vss pin. The main purposes of this capacitor are to:

- compensate voltage drops due to pulsive current sinked by the device.
- close the feedback loop of the internal voltage regulator making the system stable.

A capacitor of a value 100nF has to be connected for each couple VDD and the nearest pin Vss.

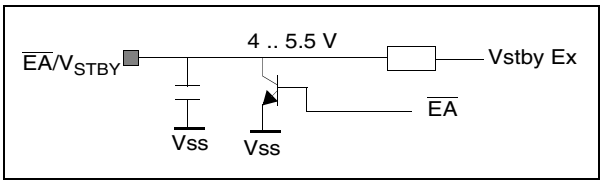
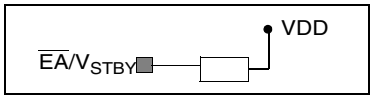
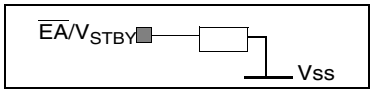
1.2 Pin V_{stby} / $\overline{EA}$

On the ST10F27x, the pin 99 provides two functionalities:

- V_{STBY} voltage(4.5 - 5.5V) applied on pin 99 maintains the RAM powered when ST10F27x main power is OFF. It must be applied before switching OFF the main power supply.
- $\overline{EA}$ functionality which configures the ST10F27x to start from external memory if its level is low during reset.

Table 1 contains the different configurations and the needed hardware for each case (if stand by mode is used or not).

Table 1. $V_{STBY}/\overline{EA}$

	$\overline{EA}$ = 1	$\overline{EA}$ = 0
Stand by mode used VSTBY = 5V when VDD is turned off		
Stand by mode not used VSTBY = 0V		

2 Clock management

Internal operation of CPU and peripherals are controlled by the same main clock named Fcpu. It is provided by the on-chip clock generator. The RTC module can be controlled either by the ST10F27x main clock or by the auxiliary 32 kHz oscillator.

2.1 Main clock control unit

The ST10F27x core and peripherals can operate with a frequency up to 64 MHz.

The ST10F27x main clock can be:

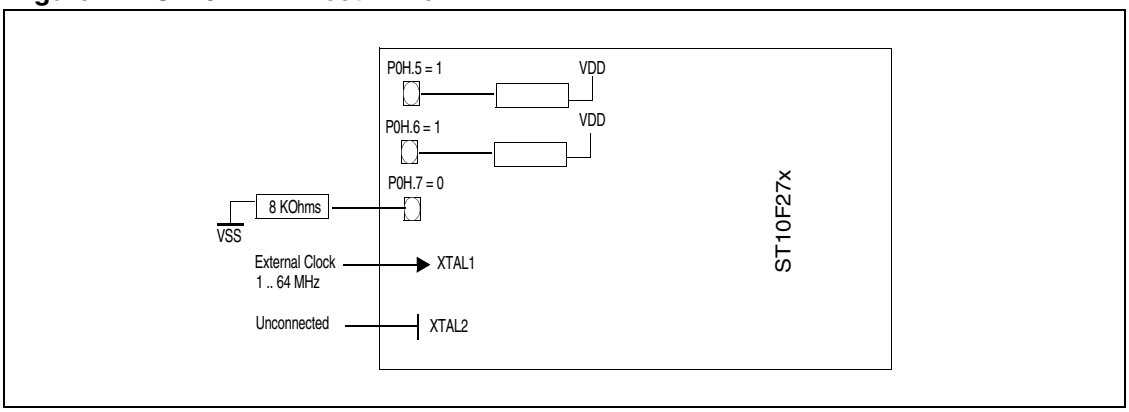
- generated using the ST10F27x internal oscillator amplifier. In this case, the input signal for the internal oscillator is generated by an external crystal or resonator with a frequency between 4MHz and 12 MHz, and is connected between XTAL1 and XTAL2: XTAL1 is the input and XTAL2 is the output. This configuration is available when using on chip PLL or the prescaler operation.
- forced by an external clock when the direct drive option is selected. In this case, the internal oscillator is disabled and neither the external crystal nor resonator is needed. The external clock is input on the XTAL1 pin of the ST10F27x and the XTAL2 pin must be left unconnected.

The clock generation mode is selected during reset according to port 0 lines: P0H.5, P0H.6, P0H.7. Each mode is described below.

2.1.1 Direct Drive operation

When pins P0H.7 = 0, P0H.6 = 1, P0H.5 = 1 during reset, the CPU clock is directly driven from the external generator connected to XTAL1 pin. In this case, neither the crystal nor the resonator is used.

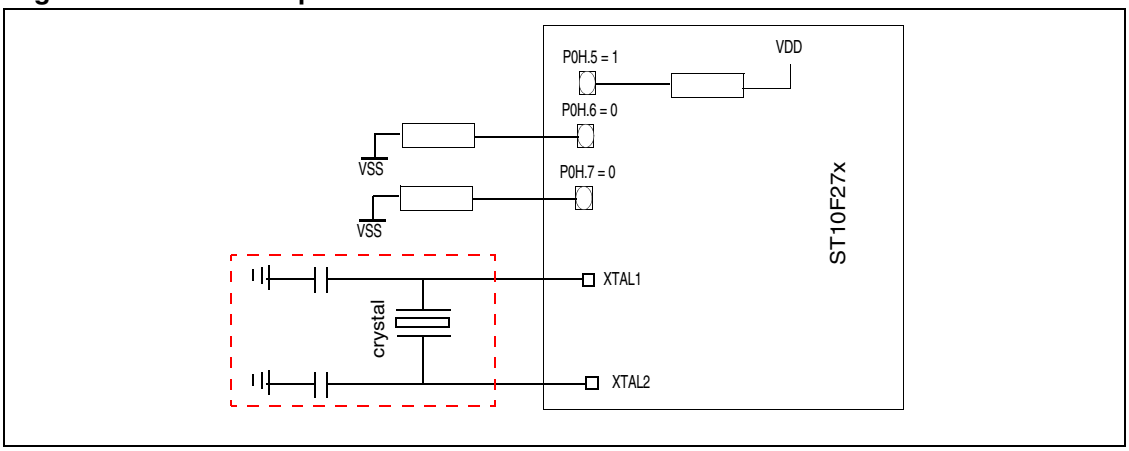
Figure 1. ST10F27x Direct Drive



2.1.2 Prescaler operation

When pins P0H.7 = 0, P0H.6 = 0, P0H.5 = 1 during reset, the CPU clock is derived from the internal oscillator amplifier. The input clock signal is generated by a crystal or a resonator with a frequency between 4MHz and 8 Mhz. The CPU frequency is equal to the input signal on pin XTAL1 divided by 2

Figure 2. Prescaler operation



For more details, please refer to the *ST10F27x datasheet*.

2.1.3 PLL operation

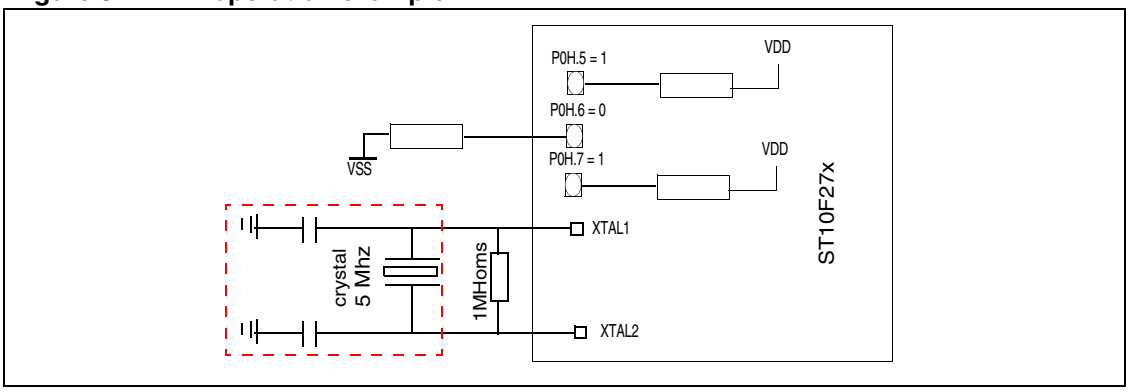
For the remaining combinations of pins P0H.7, P0H.6 and P0H.5, the PLL operation is enabled and provides the ST10F27x with a main clock. The PLL multiplies the input frequency entered on pin XTAL1 by a factor selected by the pins P0H.7, P0H.6 and P0H.5 levels.

For more details regarding the maximum crystal frequency and the resulted CPU frequency, refer to *ST10F27x datasheet*.

Example:

If a 5 Mhz external crystal is used and P0H[7..5] = 101 configuration is selected, ST10F27x will run with a 40 Mhz frequency. This example is illustrated in the following figure.

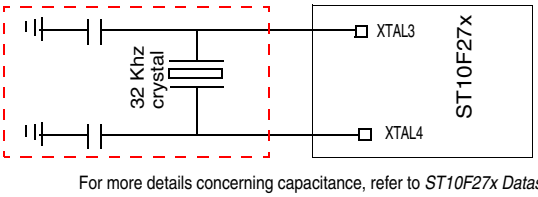
Figure 3. PLL operation example



2.2 32 kHz low power oscillator

When power down mode is entered, the main oscillator generating the ST10F27x main clock is switched OFF. If the RTC module needs to continue running during power down mode, a reference clock is needed. Therefore, a 32 kHz crystal is connected to the low power oscillator pins XTAL3 and XTAL4, in order to give a reference clock to the RTC module if the main oscillator is stopped.

Figure 4. 32 kHz oscillator



For more details concerning capacitance, refer to *ST10F27x Datasheet*

If the 32 kHz oscillator is not used, XTAL3 must be tied to ground and XTAL4 must be left unconnected.

3 Reset management

3.1 External reset circuitry

Figure 5 and *Figure 6* summarize the hardware required to operate a good reset. The first one should be used when the power down mode is not required by the application, whereas the second one shows the hardware configuration in order to use the power down mode.

Figure 5. External reset circuitry when power down mode is not used

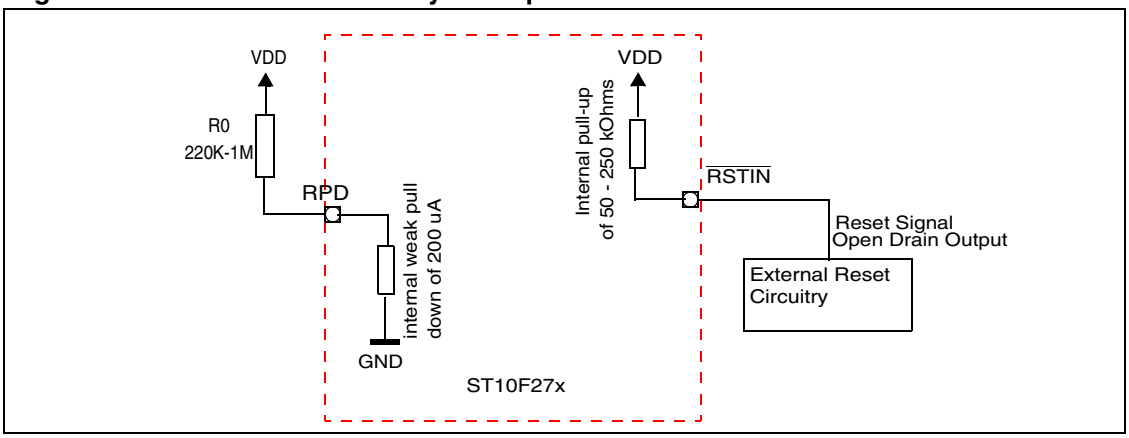
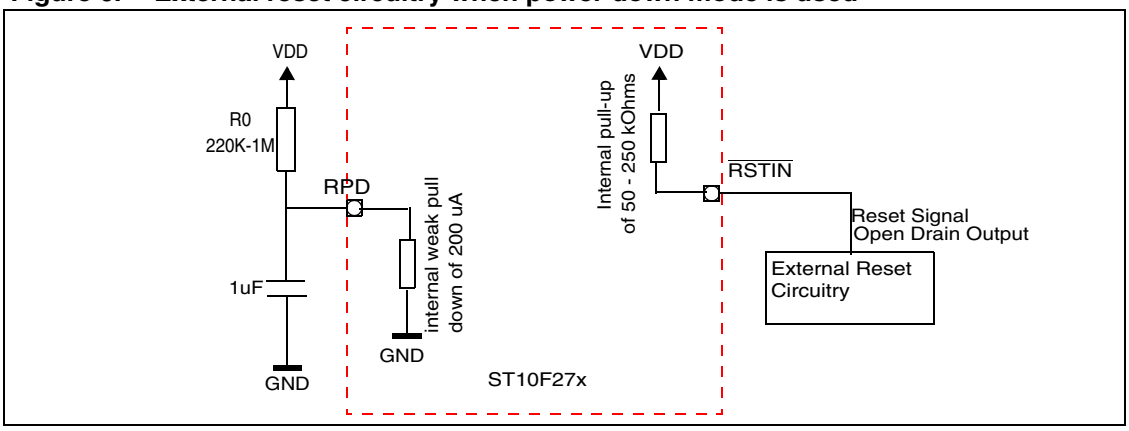


Figure 6. External reset circuitry when power down mode is used



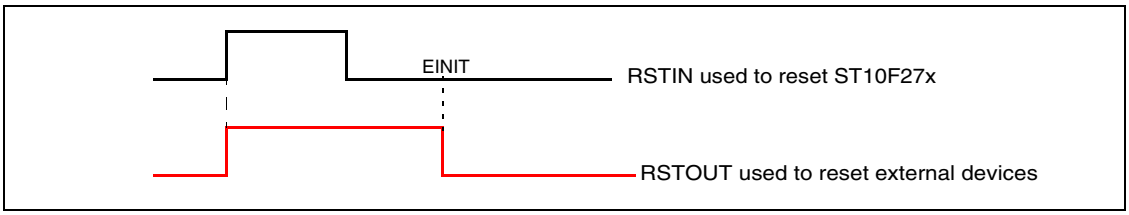
3.2 How to reset external devices with ST10F27x reset signals

If the application uses the ST10F27x with external devices, such as other microcontrollers, and if the external devices should be reset by the ST10F27x beyond the ST10 reset, there are two ways to do this:

- Using the $\overline{\text{RSTOUT}}$ pin
- Using the bidirectional reset option provided by the ST10F27x

3.2.1 $\overline{\text{RSTOUT}}$ pin

RSTOUT signal is used to reset external devices that don't need initialization before EINIT instruction of the ST10F27x. In this case, the user can execute some code before initializing the external device.



The reset circuitry on $\overline{\text{RSTIN}}$ and RPD pins used in this case is the same circuitry described in the previous section.

3.2.2 Bidirectional reset

The bidirectional reset changes $\overline{\text{RSTIN}}$ pin from a pure input to an open drain output with an integrated pull-up resistor. This mode is used:

- to convert software and watchdog resets into hardware resets
- to provide a reset signal to external devices that can't be connected to $\overline{\text{RSTOUT}}$ pin because it's maintained active during the ST10 initialization.

Pin $\overline{\text{RSTIN}}$ may be connected to external reset devices with an open drain output driver to avoid conflict.

For more details, refer to the *ST10F27x datasheet* in the section for "bidirectional reset".

4 Start up configuration

Port 0 is used to select the start up system configuration by the mean of external pull down resistors. During reset, Port 0 lines are set to input mode with internal pull up resistors. The port 0 pins are read at the end of the reset sequence.

The following table summarizes the port0 lines corresponding to the start up features:

Table 2. Port 0 fields

Port 0 lines	Function	Comments
P0L.0	Emulation mode	1)
P0L.1	Adapt mode	1)
P0L.4, P0L.5	Boot strap mode	1) See *Section 5: Boot management*
P0L.6, P0L.7	BUSTYP: CS0 Bus type configuration	1)
P0H.0	WRC Write/ Read configuration	1)
P0H.1, P0H.2	CSSEL: Chip Select	1)
P0H.3, P0H.4	SALSEL: CS0 Address Lines	1)
P0H.5.. P0H.7	CLKCFG: Clock configuration	1) See *Section 2: Clock management*

Note: 1 A low level is applied using a pull down resistor of 8 kOhms.

For more details regarding the P0 fields and corresponding meanings, refer to *ST10F27x datasheet* or *user manual*.

5 Boot management

Different boot modes are available on ST10F27x devices:

- The bootstrap mode provides a mechanism to load a program in RAM of the ST10F27x devices without using internal or external memory.
- The single chip pin $\overline{EA}$ allows the device to boot either from the internal flash or from an external memory.

5.1 Bootstrap loader

The ST10F276 provides the following boot capabilities:

- Standard bootstrap: This mode downloads a start up program of 32 bytes through the serial interface or of 128 bytes through the CAN interface after reset in the ST10F276 RAM.
- Alternate bootstrap: This mode executes a user bootstrap code written by the customer starting at address 09'0000 if some conditions are met.
- Selective bootstrap: This mode is a sub-case of the alternate bootstrap mode. It's triggered when the conditions required for the alternate bootstrap are not met.

For more details concerning the alternate bootstrap mode, please refer to the *ST10F276 user manual.*

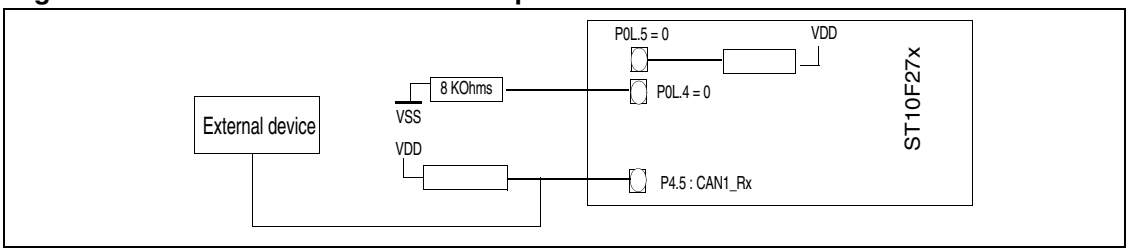
The bootstrap mode is selected according to P0L.4 and P0L.5 levels during reset.

Table 3. ST10F27x bootstrap modes

P0L.4	P0L.5	Bootstrap mode	Comments
0	1	Standard bootstrap	Use a pull up resistor on P4.5 in order to have a stable level on this pin during bootstrap via CAN. To avoid high consumption, high resistor values must be chosen. For more details please refer to the *ST10F27x user manual*
0	0	Reserved	
1	0	Alternate/Selective Bootstrap	The selection between the alternate and selective bootstrap modes is done by comparing two signatures to predefined user and alternate signatures.
1	1	User code	The ST10F27x starts fetching code form internal ROM or external ROM according to $\overline{EA}$ pin's level.

Example: The following figure illustrates the hardware required for the standard bootstrap loader via CAN interface. For more details, refer to the *ST10F27x user manual*.

Figure 7. ST10F27x Standard bootstrap via CAN



5.2 Single chip mode

If the bootstrap mode isn't activated (P0L.4 =1 & P0L.5=1) and $\overline{EA}$ = 1 during reset, the single ship mode is enabled. In this mode, the reset vector is located in the internal memory. In this case, the internal flash must contain a valid program at address 00'0000.

5.3 Boot from external memories

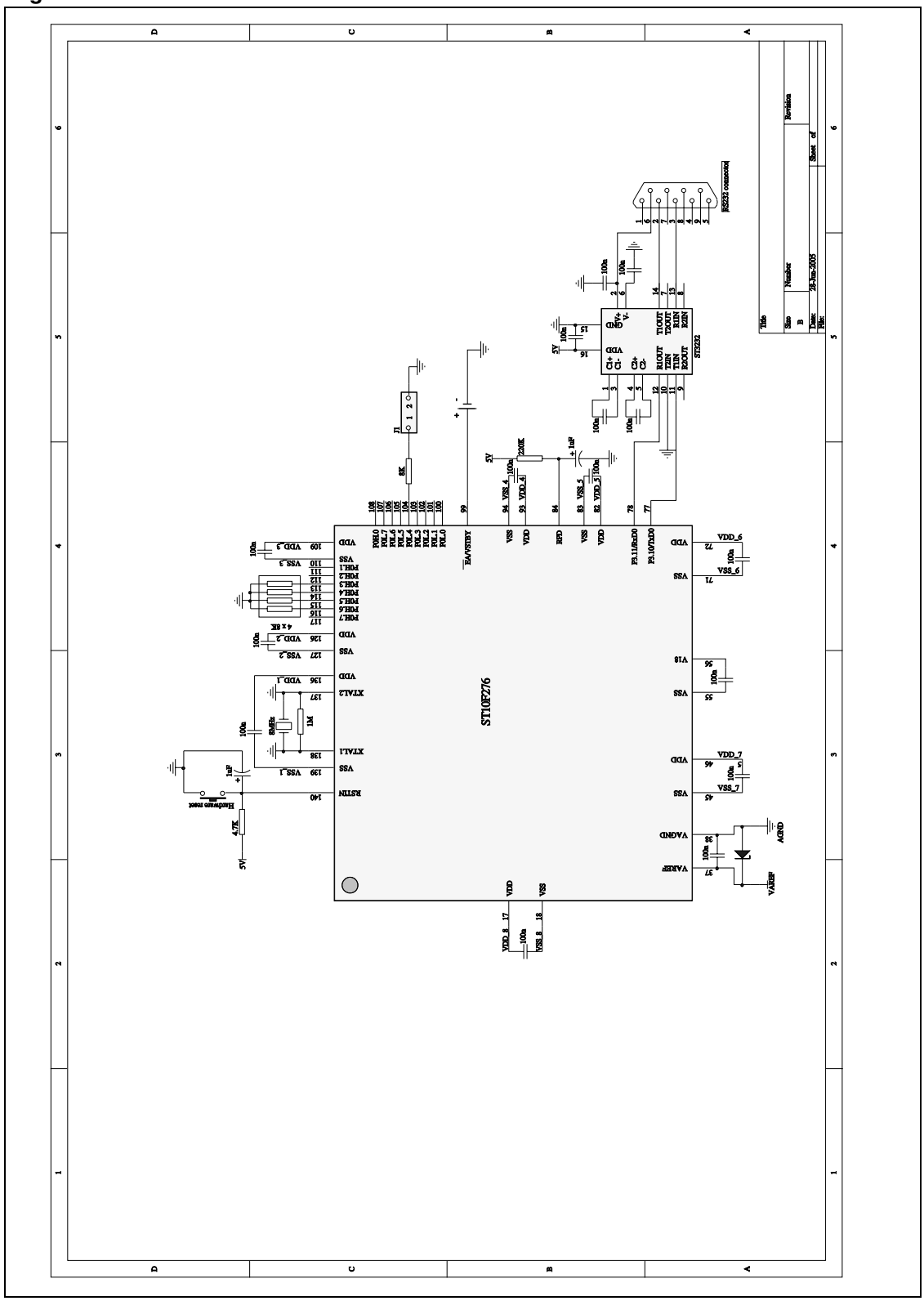
If the bootstrap mode isn't activated (P0L.4 =1 & P0L.5=1) and $\overline{EA}$ = 0, the ST10F27x will start fetching code from the external memory at address 00'0000. In this mode, the internal flash can not be accessed.

6 ST10F27x basic schematics

The schematic shown in *Figure 8* illustrates the minimum hardware requirements to get the ST10F276 running. In this example:

- The ST10F276 runs at 40MHz generated using an 8-MHz external crystal and a prescaler equal to 5 (P0H.7 = 1, P0H.6 = P0H.5 = 0 during reset). Please refer to the *Section 2: Clock management on page 4*.
- The schematic shows the ST10 in stand-alone mode, without any external memory.
- The standard bootstrap mode is activated by plugging the jumper J1 (P0L.4 = 0). As there is no external memory, the device will always boot from internal memory and $\overline{EA}$ can be forced to high level through the stand by mode RAM battery.
- RS232 comminication with a host is established using the STMicroelectronics ST3232 transciever. Please refer to its related datasheet for detailed specification.

Figure 8. ST10F27 basic schematic



7 Revision history

Date	Revision	Changes
14-Sep-2006	1	Initial release
27-Feb-2007	2	References to cancelled Application Note removed

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